REMARKS

Claims 1-6 and 8-30 remain pending in the present application. Claim 7 has been previously cancelled. Claim 1 has been amended

Claim Rejections under 35 U.S.C. § 103(a)

Claims 1-6 and 8-30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,751,983 to Abramson et al. ("Abramson") in view of U.S. Patent No. 6,065,103 to Tran et al. ("Tran").

In processor technology, when a load is predicted to be memory renamed to a previous store the prediction needs to be checked, that is, the memory renamed load is disambiguated, to determine whether the store is still in a memory ordering buffer ("MOB") when the memory renamed load retires. Since the memory renaming prediction occurs in the front-end of the processor, data consumption occurs early in the execution pipeline and the memory renamed load is not checked against the stores in the processor until the end of the execution pipeline, it is possible that the store to which the memory renamed load was predicted to forward from may have been de-allocated from the MOB. As stated in the specification, if the store has been deallocated, checking cannot be done and the memory renamed load must re-execute even if it was correct. Re-execution of the load instruction negatively impacts processor performance.

Embodiments of the present invention may be used when the store to which the memory renamed load was predicted to forward from has been de-allocated from the MOB. In accordance with an embodiment of the present invention, a trailing store buffer (TSB) may be used to maintain information from the stores that have been de-allocated from the MOB when the memory renamed load disambiguates. A generation number or color may be associated with the store information so that the memory renamed loads do not hit on younger allocated stores

(that is, stores that executed subsequent to the memory renamed load). In accordance with embodiments of the present invention, the TSB may store information for all stores that are de-allocated from the MOB or only for those stores that have memory renamed loads associated with them.

Independent claim 1 refers to a MOB to maintain a source store instruction and a TSB to maintain an address for said source store instruction, if said source store instruction has been de-allocated from the MOB. Claim 1 has been amended to bring out the feature present in the remaining independent claims that the TSB is to maintain the address to disambiguate the corresponding load instruction.

Abramson does not discuss de-allocation of the MOB or any other structure in its patent. For this structure, the Office Action relies on Tran.

Tran refers to a speculative store buffer. At Col. 2, line 60 to Col. 3, line 13, Tran discusses that increasing the size of a load/store buffer may cause problems because the logic for handling the search of entries in the load/store buffer becomes more complex and takes more time (with increasing the size of this buffer). To address this, Tran provides a speculative store buffer. A load/store unit 20 in Tran includes a load/store buffer to store memory operations corresponding to an instruction. The load/store unit also includes the speculative store buffer 44 that stores a speculative state of one or more memory locations. In other words, as described at Col. 5, lines 37-52, the speculative store buffer stores an address for a memory location and a speculative state for that memory location. The speculative state is based on one or more store memory operations affecting a given memory location. Accordingly, when doing dependency checking for a load memory operation, an address lookup is performed in the speculative store buffer 44, and if there is a hit, then the speculative state of the memory location is forwarded. If there is a miss, then the data cache 14 is accessed for the non-speculative state of a memory operation. (Col. 5, lines 53-65).

As each speculative store memory operation is processed, a hit in the speculative store buffer results in an update for the speculative state for the appropriate memory location. If there is a miss, then a storage location is allocated for that memory location and updated accordingly (Col. 9, lines 22-45).

The Office Action cites Col. 11, lines 1-8 as showing the Tran discloses "a trailing store buffer to maintain an address for said store instruction, if said store instruction has been de-allocated from said memory ordering buffer." For convenience, the cited text is provided below:

> For non-speculative store memory operations, the store memory operation is conveyed to both speculative store buffer 44 and data cache 14. If the store memory operation has not previously accessed speculative store buffer 44 and speculative store buffer 44 detects a hit for the store memory operation, speculative store buffer 44 may update the hitting location with the store data (under the control of control unit 42). On the other hand, since data cache 14 is being updated with the store data as well, speculative store buffer 44 may invalidate the hitting location (under the control of control unit 42).

It is presumed that the Office Action is equating the load/store buffer 40 as the memory ordering buffer of the pending claims. The cited section above does not discuss the allocation or deallocation of the load/store buffer 40. It is not clear how the above has any relevance to de-allocation from a memory ordering buffer. The cited section states that a non-speculative store memory operation will be used to update the cache 14 and to update the speculative store buffer 44. Alternatively, the speculative store buffer may invalidate the speculative value for the relevant memory location. There is nothing in this section about deallocation from a memory ordering buffer and the maintenance of an address for a store instruction if there is a deallocation.

CONCLUSION

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
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Tran does not describe maintaining an address for the source store instruction if the source store instruction has been de-allocated from the memory ordering buffer. In Tran, store instructions are retained in the load/store buffer until they are non-speculative and the corresponding entry in the speculative store buffer 44 is invalidated (see Col. 12, lines 30-35). Also, note at Col. 11, lines 17-19, Tran states that "[s]ince data cache 14 is being updated concurrently, it may be desirable not to allocate a speculative store buffer 44 storage location." Such implies that there is no need to create a storage location in the storage buffer 44 for a non-speculative store memory operation. Accordingly, Tran does not teach maintaining an address in the speculative store buffer if the source instruction has been de-allocated as set forth in the Office Action.

Since features of the claims are neither taught nor suggested by Abramson. Reconsideration and withdrawal of the rejection of claims 1-6 and 8-30 under 35 U.S.C. § 103(a) is respectfully requested.